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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,270	12/30/2003	Saikumar Jayaraman	884.888US1	7480
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INTEL CORPORATION c/o INTELLEVATE, LLC P.O. BOX 52050 MINNEAPOLIS, MN 55402			EXAMINER LIGHTFOOT, ELENA TSOY	
			ART UNIT 1792	PAPER NUMBER
			MAIL DATE 08/27/2008	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/751,270

**Applicant(s)**

JAYARAMAN, SAIKUMAR

**Examiner**

Elena Tsoy Lightfoot

**Art Unit**

1792

**Period for Reply** -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 17 July 2008.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1, 2, 14-24 and 31-36 is/are pending in the application.
- 4a) Of the above claim(s) 21-24 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12, 14-20 and 31-36 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
- Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(c), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(c) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 17, 2008 has been entered.

***Response to Amendment***

Amendment filed on July 17, 2008 has been entered. Claims 1-12, 14-24, and 31-36 are pending in the application. Claims 21-24 are withdrawn from consideration as directed to a non-elected invention.

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 2, 4, 5, 7, 10-12, 14, 15, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of West et al (US 4828965), further in view of Suda et al (US 4731855) and Kamieniecki et al (US 5661408).

Jacobson et al is applied here for the same reasons as set forth in paragraph 8 of the Office Action mailed on 7/26/2007.

As to Amendment, Jacobson et al teaches that their method may be advantageously used for fabrication of finely featured *electronic and electromechanical* components (See column 1, lines 14-16) instead of prior art techniques such as *microlithography* (See column 1, lines 18), photolithography (See column 1, lines 44-45), "*nanoimprint lithography*" (See column 1, lines 46-47). Therefore, it would have been obvious to one of ordinary skill in the art at the time the

invention was made to have used the method of Jacobson et al for fabrication of any finely featured electronic and electromechanical components that would require *microlithography* or nanoimprint lithography techniques since Jacobson et al does not limit its teaching to fabrication of particular electronic and electromechanical components.

Jacobson et al fails to teach that the electronic and electromechanical components fabrication of which require prior art techniques such as *microlithography*, photolithography, "nanoimprint lithography include printed wiring board (PWB) (Claim 1).

However, West et al teaches that *microlithography* processes are used for making miniaturized electronic components such as in the fabrication of integrated circuits and *printed wiring board* circuitry (See column 1, lines 13-15) wherein a thin coating or film of a photoresist composition is first applied to a substrate material, such as silicon wafers used for making integrated circuits or aluminum lithographic printing plates or copper plates of printed wiring boards (See column 1, lines 13-33).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the method of Jacobson et al for fabrication of PWB instead of microlithography since Jacobson et al does not limit its teaching to fabrication of particular electronic and electromechanical components.

As to in situ testing, Jacobson et al in view of West et al fails to teach *in situ* testing the substrate while attached as part of an array of substrates.

Suda et al teach that it is essential to check whether any defect is included in or any foreign material is deposited on a pattern formed on a *semiconductor wafer* in order to improve the yield in the manufacture of a *semiconductor device* (See column 1, lines 15-18) in the course of a production line without taking out the semiconductor device from the line; that is, they are not applicable to a process in-line test (See column 1, lines 50-57).

Kamieniecki et al teach that frequently, failure of an individual operation is detected only after the completion of the entire, very expensive, process of IC fabrication. Due to the very high cost of advanced IC fabrication processes, such failures result in the severe financial losses to the integrated circuit manufacturer. Therefore detection of errors in the manufacturing process, immediately after their occurrence, i.e. real-time in-line testing of semiconductor wafers during integrated circuit fabrication (See column 1, lines 5-9) allows to prevent the unnecessary

continuation of the fabrication of devices which are destined to malfunction, and hence, could substantially reduce the financial losses resulting from such errors. See column 1, line 5 to column 2, line 24.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have conducted real-time in-line testing of substrates during the manufacture of PWB in Jacobson et al in view of West et al without taking out PWB from the line with the expectation of reducing the financial losses resulting from errors, as taught by Suda et al and Kamieniecki et al.

3. Claims 1, 2, 4-12, 14-20, and 31-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Carter (US 6,730,617) in view of Suda et al and Kamieniecki et al for the reasons of record set forth in paragraph 5 of the Office Action mailed on 10/09/2007 because the amendment does not change the scope of claimed invention.

4. Claims 3, 6, 20, 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of West et al, further in view of Suda et al and Kamieniecki et al, as applied above, and further in view of Bulthaup et al (US 6,936,181) for the reasons of record set forth in paragraph 10 of the Office Action mailed on 7/27/2006.

5. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of West et al, further in view of Suda et al and Kamieniecki et al, or over Carter in view of Suda et al and Kamieniecki et al, as applied above, and further in view of Walter et al (US 4,099,913) for the reasons of record set forth in paragraph 9 of the Office Action mailed on 7/27/2006.

6. Claims 6, 8, 9, 16, 20, 31-32, and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson et al in view of West et al, further in view of Suda et al and Kamieniecki et al, as applied above, and further in view of Carter for the reasons of record set forth in paragraph 12 of the Office Action mailed on 7/27/2006.

#### ***Response to Arguments***

7. Applicant's arguments filed July 17, 2008 have been fully considered but they are not persuasive.

§103 Rejection of the Claims

Jacobson et al or Carter in view of Suda et al. and Kamieniecki et al.

Appellants argue that Suda and Kamieniecki do not remedy neither Jacobson nor Carter because Jacobson's or Carter's technology if applied to either of Suda or Kamieniecki, would destroy such inventions. Further, the "substrate" of Jacobson is not the "substrate" of either of Suda or Kamieniecki. Consequently, merely that of either of Suda or Kamieniecki may teach testing of their substrates, fails to show a teaching or suggestion to combine their technologies with Jacobson. Further, Jacobson or Carter would not look to either of Suda or Kamieniecki to solve any technical challenges or fields of endeavor.

The Examiner respectfully disagrees with this argument. First of all, Suda and Kamieniecki were cited by the Examiner only to show that **in-line or in-situ testing was known in the art** of manufacturing semiconductor devices for e.g. *fast testing of patterns on semiconductor wafers, etc. to reduce the financial losses resulting from errors*. The Examiner never addressed the testing techniques because they were not recited in claims. Therefore, in contrast to Applicants assertion, neither Jacobson's/Carter's technology was applied to either Suda or Kamieniecki nor testing techniques of Suda or Kamieniecki were applied to Jacobson.

Second, one of ordinary skill in the art would have *reasonable expectation of success* in reducing the financial losses resulting from errors fast testing of patterns on *various* substrates.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elena Tsoy Lightfoot whose telephone number is 571-272-1429. The examiner can normally be reached on Monday-Friday, 9:00AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

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system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Elena Tsoy Lightfoot, Ph.D.  
Primary Examiner  
Art Unit 1792

August 26, 2008

/Elena Tsoy Lightfoot/